ABSTRACT

A semiconductor memory using a DLL circuit having a phase comparison circuit for comparing phases of an internal clock and a delay clock and a variable delay addition circuit for adjusting delay amount according to a signal from the phase comparison circuit comprises a means for inputting a first signal latched to a logic "1" by start of one clock cycle of the internal clock to the variable delay addition circuit through a dummy delay at the start of burst and a means for detecting the duration time of the logic "1" of the first signal inputted by the variable delay addition circuit through the dummy delay until one clock cycle of the internal clock is completed and setting the initial value of delay amount of the variable delay addition circuit based on the duration time.